Academic Course Description

BHARATH UNIVERSITY
Faculty of Engineering and Technology
Department of Electronics and Communication Engineering

BEC702 Digital CMOS VLSI

Seventh Semester (2017-2018) Odd semester

Course (catalog) description

CMOS is important to learn as it is a basic integrated circuit technology due to its low power (at moderate frequencies), good scalability, and rail-to-rail operation. In this course, the reader is systematically introduced to the entire range of CMOS circuit design, starting with individual CMOS, basic circuit building blocks, and broad view of both combinational and sequential circuits.

Compulsory/Elective course: Compulsory for ECE students

Credit & contact hours : 4 & 60

Course Coordinator : Ms.M.Jasmin, Assoc. Professor.

Instructor(s) :

Name of the instructor	Class handling	Office location	Office phone	Email (domain: @bharathuniv.ac.in)	Consultation
Ms.M.Jasmin	IV	SA 006		jasmine.ece	12.30 -1.30 PM

Relationship to other courses

Pre – requiste : Principles of Digital Electronics

Assume Knowledge : Basic knowledge in Digital System Design and Electronic circuits

Following courses : Nil

Syllabus Contents

UNIT I INTRODUCTION TO MOS TRANSISTOR 12HOURS

MOS Fabrication**,** Enhancement mode and Depletion mode MOSFET, ,Threshold voltage derivation – body effect – Drain current Vs voltage derivation – channel length modulation – CMOS technologies, CMOS Fabrication: n-well – p-well – twin tub –DC transfer characteristics

UNIT II MOS CIRCUITS DESIGN PROCESS AND CMOS LOGIC GATES 12HOURS

MOS Layers, Stick Diagram, Layout Diagram, Propagation Delays, CMOS Static Logic Transmission Gate Logic, Tri-State Logic , Pass Transistor Logic , Dynamic CMOS Logic , Domino CMOS Logic,., Differential Cascade Voltage Switch (DCVS) Logic, Scaling of MOS Circuits.

UNIT III VLSI IMPLEMENTATION STRATEGIES 12HOURS

Introduction – Design of Adders: carry look ahead-carry select-carry save.Design of multipliers: Array – Braun array – Baugh-Wooley Array.Introduction to FPGA – Full custom and Semi custom design, Standard cell design and cell libraries, FPGA building block architectures

UNIT IV CMOS TESTING

12HOURS

Need for testing- Testers, Text fixtures and test programs- Logic verification- Silicon debug principles- Manufacturing test – Design for testability – Boundary scan

UNIT V SPECIFICATION USING VERILOG HDL 12HOURS

Basic concepts- identifiers- gate primitives, gate delays, operators, timing controls, procedural assignments conditional statements, Data flow and RTL, structural gate levelswitch level modeling, Design hierarchies, Behavioral and RTL modeling, Test benches, Design of decoder, equality detector, comparator, priorityencoder, half adder, full adder, Ripple carry adder, D latch and D flip flop

Text book(s) and/or required materials

TEXT BOOKS

T1. Weste and Harris: CMOS VLSI DESIGN (Third edition) Pearson Education, 2005
T2. Uyemura J.P: Introduction to VLSI circuits and systems, Wiley 2002.

REFERENCES

R1 D.A Pucknell & K.Eshraghian Basic VLSI Design, Third edition, PHI,2003
R2 Wayne Wolf, Modern VLSI design, Pearson Education, 2003
R3 M.J.S.Smith: Application specific integrated circuits, Pearson Education,1997
R4 J.Bhasker: Verilog HDL primer, BS publication,2001
R5 Ciletti Advanced Digital Design with the Verilog HDL, Prentice Hall of India, 2003
R6. *https://en.wikipedia.org/wiki/Very-large-scale_integration*

Computer usage: To model a Combinational circuit and Sequential circuit using hardware description language Verilog HDL and validate its functionality.

Professional component

General	-	0%
Basic Sciences	-	0%
Engineering sciences & Technical arts	-	0%
Professional subject	-	100%

Broad area : Communication | Signal Processing | **Electronics** | VLSI | Embedded

Test Schedule

S. No.	Test	Tentative Date	Portions	Duration
1	Cycle Test-1	August 1st Week	Session 1 to 18	2 Periods
2	Cycle Test-2	September 2nd Week	Session 19 to 36	2 Periods
3	Model Test	October 2nd Week	Session 1 to 60	3 Hrs
4	University Examination	TBA	All sessions / Units	3 Hrs.

Mapping of Instructional Objectives with Program Outcome

Learn about the concepts starting with individual CMOS, basic circuit building blocks, and broad view of both combinational and sequential circuits.	Correlates to program outcome		
	H	M	L
1. To learn about IC fabrication, MOS transistor action and its parameters.	h	a,i	-
2. Express the Layout of simple MOS circuit using Lambda based design rules.	c,i,j	a,h	-
3. About the implementation of various adders and multipliers in VLSI technology. .	d,j,k	a,c	-
4. About the design styles of FPGA.	e,j	a,h	-
5. About testing of CMOS circuits.	b,i	-	-
6.To understand the concepts of modeling a digital system using Hardware Description Language.	a,e,k	-	-

H: high correlation, M: medium correlation, L: low correlation

Draft Lecture

Session	Topics	Problem Solving (Yes/No)	Text / Chapter
UNITI : INTRODUCTION TO MOS TRANSISTOR			
1,2	MOS Fabrication	No	R1-Chapter 1
3	Enhancement mode and Depletion mode MOSFET	No	T1-Chapter 2
4	Threshold voltage derivation	No	
5	Drain current Vs voltage derivation	No	
6	channel length modulation	No	
7	CMOS technologies	No	
8	n-Well Process	No	R1-Chapter 1
9	p-well Process	No	
10	Twin tub Process	No	
11,12	Dc transfer characteristics	No	T1-Chapter 2
UNIT II MOS CIRCUITS DESIGN PROCESS AND CMOS LOGIC GATES			
13,14	Stick Diagram	No	R1-Chapter 3
15,16	Layout Diagram	No	
17	Propagation Delays	No	T1-Chapter 6
18	CMOS Static Logic	No	
19	Transmission Gate Logic	No	
20	Tri-State Logic	No	
21	Pass Transistor Logic , Dynamic CMOS Logic	No	
22	Domino CMOS Logic,., Differential Cascade Voltage Switch (DCVS) Logic	No	
23,24	Scaling of MOS Circuits.	No	R1-Chapter 5
UNIT III VLSI IMPLEMENTATION STRATEGIES			
25	Design of Adders: carry look ahead	No	R1-Chapter 8
26	carry select and carry save adders	No	
27	Design of Array multipliers	No	
28	Braun array multiplier	No	
29	Baugh-Wooley Array	No	
30	Introduction to FPGA	No	R3 –Chapter 1
31	Full custom and Semi custom design	No	
32,33	Standard cell design and cell libraries	No	
34,35	FPGA building block architectures	No	
36	Summary and Quiz on Unit III	No	
UNITIV- CMOS TESTING			
37,38	Need for testing	**No**	T1 –Chapter 12
39	Testers, Text fixtures	No	
40	test programs	No	
41,42	Logic verification	No	
43	Silicon debug principles	No	

44	Manufacturing test	No	
45	Design for testability	No	
46,47	Boundary scan	No	
48	Summary and Quiz on Unit III	No	
UNIT-V- SPECIFICATION USING VERILOG HDL			
49	Design Hierarchies	No	R4 Chapter 1,2,5
50	Basic concepts	No	
51	gate delays, operators, timing controls	No	
52,53	procedural assignments conditional statements	No	
54	Data Flow Modeling	No	
55	Gate Level Modeling	No	
56	Switch Level Modeling	No	
57	Structural Level Modeling	No	
58,59,60	Design of combinational and Sequential Logic circuits circuits in all types of modeling	No	

Teaching Strategies

The teaching in this course aims at establishing a good fundamental understanding of the areas covered using:

- Formal face-to-face lectures
- Tutorials which allow the students to gain knowledge in programming of Digital System logic using Verilog.
- Laboratory sessions, which support the formal lecture material and also develop the programming
- skill of the students
- Small periodic quizzes, to enable you to assess your understanding of the concepts.

Evaluation Strategies

Cycle Test – I	-	5%
Cycle Test – II	-	5%
Model Test	-	10%
Assignment /Seminar/online test/quiz	-	5%
Attendance	-	5%
Final exam	-	70%

Prepared by: **M.Jasmin,** Assoc Professor ,Department of ECE **Dated :**

Addendum

ABET Outcomes expected of graduates of B.Tech / ECE / program by the time that they graduate*:*

a. An ability to apply knowledge of mathematics, science, and engineering

b. An ability to design and conduct experiments, as well as to analyze and interpret data

c. An ability to design a hardware and software system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability

d. An ability to function on multidisciplinary teams

e. An ability to identify, formulate, and solve engineering problems

f. An understanding of professional and ethical responsibility

g. An ability to communicate effectively

h. The broad education necessary to understand the impact of engineering solutions in a global, economic, environmental, and societal context

i. A recognition of the need for, and an ability to engage in life-long learning

j. A knowledge of contemporary issues

k. An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice.

Program Educational Objectives

PEO1: PREPARATION

Electronics Engineering graduates are provided with a strong foundation to passionately apply the fundamental principles of mathematics, science, and engineering knowledge to solve technical problems and also to combine fundamental knowledge of engineering principles with modern techniques to solve realistic, unstructured problems that arise in the field of Engineering and non-engineering efficiently and cost effectively.

PEO2: CORE COMPETENCE

Electronics engineering graduates have proficiency to enhance the skills and experience to apply their engineering knowledge, critical thinking and problem solving abilities in professional engineering practice for a wide variety of technical applications, including the design and usage of modern tools for improvement in the field of Electronics and Communication Engineering.

PEO3: PROFESSIONALISM

Electronics Engineering Graduates will be expected to pursue life-long learning by successfully participating in post graduate or any other professional program for continuous improvement which is a requisite for a successful engineer to become a leader in the work force or educational sector.

PEO4: SKILL

Electronics Engineering Graduates will become skilled in soft skills such as proficiency in many languages, technical communication, verbal, logical, analytical, comprehension, team building, interpersonal relationship, group discussion and leadership ability to become a better professional.

PEO5: ETHICS

Electronics Engineering Graduates are morally boosted to make decisions that are ethical, safe and environmentally-responsible and also to innovate continuously for societal improvement.

Course Teacher	Signature
Ms M.Jasmin	

Course Coordinator **HOD/ECE**